



8-Channel, Dual 4-Channel, Triple 2-Channel Multiplexers, with 0.5 pC Charge Injection

DESCRIPTION

The DG4051A, DG4052A and DG4053A are precision low voltage, single and dual supply CMOS analog multiplexers. The DG4051A is an 8-channel multiplexer, the DG4052A is a dual 4-channel multiplexer and the DG4053A is a triple 2-channel multiplexer or triple SPDT.

They are designed to operate from a +2.7 V to +12 V single supply or from ±2.5 V to ±5 V dual supplies and are fully specified at +3 V, +5 V and ±5 V. All control logic inputs have guaranteed 2.0 V high limit when operating from +5 V or ±5 V supplies and 1.4 V when operating from a +3 V supply.

The DG4051A, DG4052A and DG4053A switches conduct equally well in both directions, offer rail to rail analog signal handling and can be used both as multiplexers as well as de-multiplexers.

< 0.5 pC low charge injection coupled with very low switch capacitance make these products ideal for precision instrumentation multiplexers.

Operating temperature is specified from -40 °C to +125 °C.

The DG4051A, DG4052A and DG4053A are available in 16 lead SOIC, TSSOP and the space saving 1.8 x 2.6 mm miniQFN packages.

FEATURES

- +2.7 V to +12 V single supply operation
- ±2.5 V to ±5 V dual supply operation
- Fully specified at +3 V, +5 V, ±5 V
- 100 Ω maximum on-resistance
- Low voltage, 2.5 V CMOS/TTL compatible
- Low charge injection (< 0.5 pC typ.)
- High bandwidth: 330 MHz to 700 MHz
- Low switch capacitance (C_{S(off)} 3 pF typ.)
- Excellent isolation and crosstalk performance (typ. 47 dB at 100 MHz)
- 16 pin SOIC, TSSOP and miniQFN package (1.8 x 2.6 mm)
- Fully specified from -40 °C to +85 °C and -40 °C to +125 °C

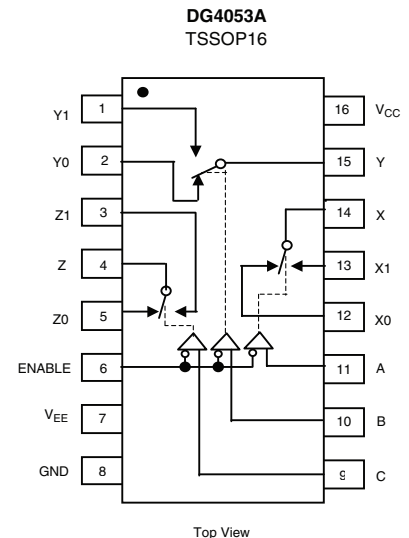
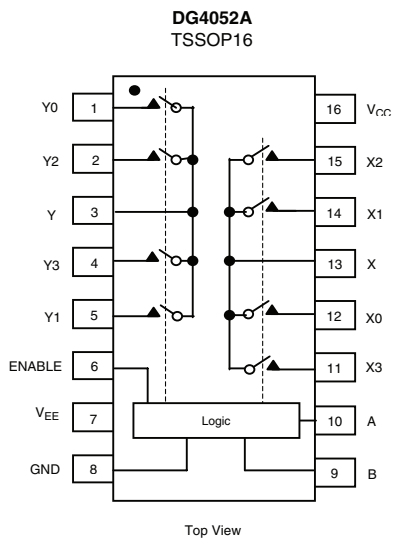
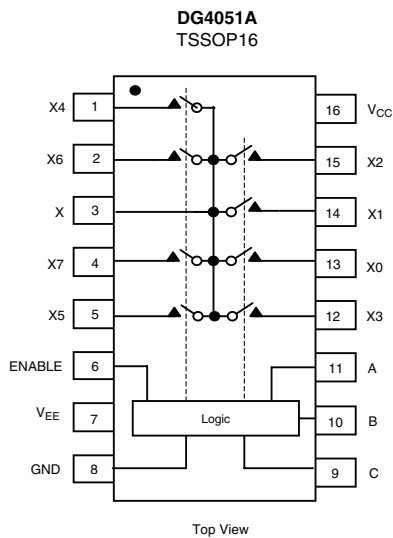


RoHS COMPLIANT

APPLICATIONS

- Precision instrumentation
- Sample and hold applications
- Medical instruments
- High speed communication applications
- Automated test equipment
- High-end data acquisition

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



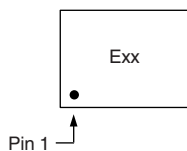
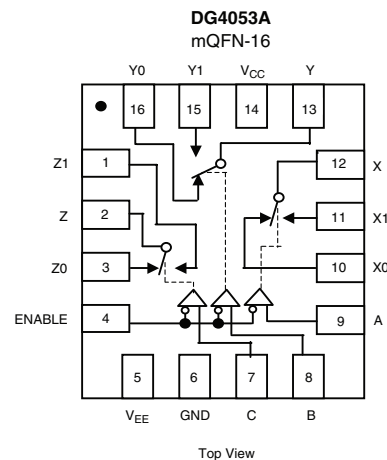
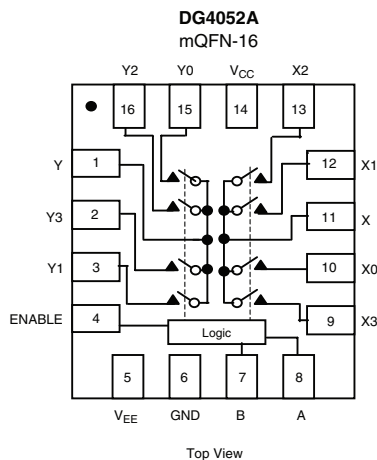
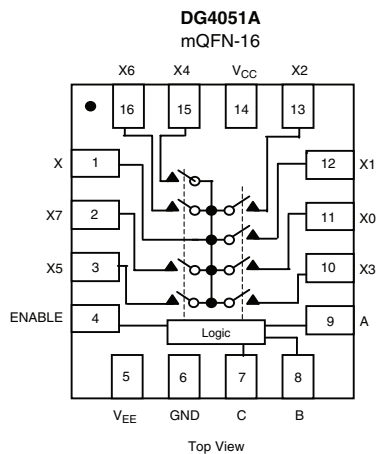
ENABLE = LO, all switches are controlled by addr pins.
ENABLE = HI, all switches are off.

DG4051A/DG4052A/DG4053A



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FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: Exx for DG4051A (miniQFN16) Fxx for DG4052A Gxx for DG4053A
xx = Date/Lot Traceability Code

TRUTH TABLE						
Enable Input	Select Inputs			On Switches		
	C	B	A	DG4051A	DG4052A	DG4053A
H	X	X	X	All Switches Open	All Switches Open	All Switches Open
L	L	L	L	X to X0	X to X0, Y to Y0	X to X0, Y to Y0, Z to Z0
L	L	L	H	X to X1	X to X1, Y to Y1	X to X1, Y to Y0, Z to Z0
L	L	H	L	X to X2	X to X2, Y to Y2	X to X0, Y to Y1, Z to Z0
L	L	H	H	X to X3	X to X3, Y to Y3	X to X1, Y to Y1, Z to Z0
L	H	L	L	X to X4	X to X0, Y to Y0	X to X0, Y to Y0, Z to Z1
L	H	L	H	X to X5	X to X1, Y to Y1	X to X1, Y to Y0, Z to Z1
L	H	H	L	X to X6	X to X2, Y to Y2	X to X0, Y to Y1, Z to Z1
L	H	H	H	X to X7	X to X3, Y to Y3	X to X1, Y to Y1, Z to Z1

ORDERING INFORMATION		
Temp Range	Package	Part Number
DG4051A/4052A/4053A		
- 40 °C to 125 °C ^a	16-Pin TSSOP	DG4051AEQ-T1-E3 DG4052AEQ-T1-E3 DG4053AEQ-T1-E3
	16-Pin miniQFN	DG4051AEN-T1-E4 DG4052AEN-T1-E4 DG4053AEN-T1-E4

Notes:

a. - 40 °C to 85 °C datasheet limits apply.



ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted			
Parameter	Limit	Unit	
V+ to V-	14	V	
GND to V-	7		
Digital Inputs ^a , V_S , V_D	(V-) - 0.3 to (V+) + 0.3 or 30 mA, whichever occurs first		
Continuous Current (Any Terminal)	30	mA	
Peak Current, S or D (Pulsed 1 ms, 10 % Duty Cycle)	100		
Storage Temperature	- 65 to 150	$^\circ\text{C}$	
Power Dissipation ^b	16-Pin TSSOP ^c	450	mW
	16-Pin miniQFN ^{d, e}	525	
Thermal Resistance ^b	16-Pin TSSOP	178	C/W
	16-Pin miniQFN ^e	152	

Notes:

- a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 5.6 mW/ $^\circ\text{C}$ above 70 $^\circ\text{C}$.
- d. Derate 6.6 mW/ $^\circ\text{C}$ above 70 $^\circ\text{C}$.
- e. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS FOR DUAL SUPPLIES									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{CC} = +5\text{ V}$, $V_{EE} = -5\text{ V}$ $V_{IN(A, B, C \text{ and } ENABLE)} = 2.0\text{ V}$, 0.8 V^a	Temp. ^b	Typ. ^c	- 40 to 125 $^\circ\text{C}$		- 40 to 85 $^\circ\text{C}$		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		- 5	5	- 5	5	V
On-Resistance	R_{ON}	$I_S = 1\text{ mA}$, $V_D = -3\text{ V}$, 0 V , $+3\text{ V}$	Room Full	66		100 125		100 118	Ω
On-Resistance Match	ΔR_{ON}	$I_S = 1\text{ mA}$, $V_D = \pm 3\text{ V}$	Room Full	3		6 10		6 8	
On-Resistance Flatness	$R_{FLATNESS}$	$I_S = 1\text{ mA}$, $V_D = -3\text{ V}$, 0 V , $+3\text{ V}$	Room Full	7.9		12 16		12 14	
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 5.5\text{ V}$, $V_- = -5.5\text{ V}$, $V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$	Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	nA
	$I_{D(off)}$		Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	
Channel On Leakage Current	$I_{D(on)}$	$V_+ = 5.5\text{ V}$, $V_- = -5.5\text{ V}$, $V_S = V_D = \pm 4.5\text{ V}$	Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	$V_{IN(A, B, C \text{ and } ENABLE)}$ Under Test = 0.8 V	Full	0.01	- 1	1	- 1	1	μA
Input Current, V_{IN} High	I_{IH}	$V_{IN(A, B, C \text{ and } ENABLE)}$ Under Test = 2.0 V	Full	0.01	- 1	1	- 1	1	
Input Capacitance ^e	C_{IN}	$f = 1\text{ MHz}$	Room	3.4					pF
Dynamic Characteristics									
Off Isolation	OIRR	$R_L = 50\ \Omega$, $C_L = 1\text{ pF}$	Room	f = 10 MHz	67				dB
				f = 100 MHz	46				
Channel-to-Channel Crosstalk	X_{TALK}		f = 10 MHz	Room	67				
			f = 100 MHz	Room	47				
Bandwidth, 3dB	BW	$R_L = 50\ \Omega$	Room	DG4051A	330				MHz
			Room	DG4052A	450				
			Room	DG4053A	730				



SPECIFICATIONS FOR DUAL SUPPLIES									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{CC} = +5\text{ V}$, $V_{EE} = -5\text{ V}$ $V_{IN(A, B, C \text{ and } ENABLE)} = 2.0\text{ V}$, 0.8 V^a	Temp. ^b	Typ. ^c	- 40 to 125 °C		- 40 to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Dynamic Characteristics									
Transition Time	t_{TRANS}	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ See Figure 1, 2, 3	Room Full	36		110 127		110 117	ns
Enable Turn-On Time	t_{ON}		Room Full	31		108 119		108 114	
Enable Turn-Off Time	t_{OFF}		Room Full	29		92 103		92 98	
Break-Before-Make Time Delay	t_D		Room Full	6		2		2	
Charge Injection ^e	Q	$V_g = 0\text{ V}$, $R_g = 0\ \Omega$, $C_L = 1\text{ nF}$	Room	0.25					pC
Off Isolation ^e	OIRR	$R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ $f = 100\text{ kHz}$	Room	< - 90					dB
Channel-to-Channel Crosstalk ^e	X_{TALK}		Room	< - 90					
Source Off Capacitance ^e	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	3					pF
Drain Off Capacitance ^e	$C_{D(off)}$		Room	12					
Channel On Capacitance ^e	$C_{D(on)}$		Room	17					
Total Harmonic Distortion ^e	THD	Signal = 5 V_{RMS} , 20 Hz to 20 kHz, $R_L = 600\ \Omega$	Room	0.28					%
Power Supplies									
Power Supply Current	I_+	$V_{CC} = +5\text{ V}$, $V_{EE} = -5\text{ V}$ $V_{IN(A, B, C \text{ and } ENABLE)} = 0\text{ or }5\text{ V}$	Room Full	0.05		1 10		1 10	μA
Negative Supply Current	I_-		Room Full	- 0.05	- 1 - 10		- 1 - 10		
Ground Current	I_{GND}		Room Full	- 0.05	- 1 - 10		- 1 - 10		



SPECIFICATIONS FOR UNIPOLAR SUPPLIES									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{CC} = +5\text{ V}$, $V_{EE} = 0\text{ V}$ $V_{IN(A, B, C \text{ and } ENABLE)} = 2.0\text{ V}$, 0.8 V^a	Temp. ^b	Typ. ^c	- 40 to 125 °C		- 40 to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	5	0	5	V
On-Resistance	R_{ON}	$I_S = 1\text{ mA}$, $V_D = 0\text{ V}$, $+3.5\text{ V}$	Room Full	107		165 205		165 194	Ω
On-Resistance Match	ΔR_{ON}	$I_S = 1\text{ mA}$, $V_D = +3.5\text{ V}$	Room Full	3.2		8 13		8 11	
On-Resistance Flatness	$r_{FLATNESS}$	$I_S = 1\text{ mA}$, $V_D = 0\text{ V}$, $+3\text{ V}$	Room Full	8.2		17 21		17 19	
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = +5.5\text{ V}$, $V_- = 0\text{ V}$ $V_D = 1\text{ V}/4.5\text{ V}$, $V_S = 4.5\text{ V}/1\text{ V}$	Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	nA
	$I_{D(off)}$		Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	
Channel On Leakage Current	$I_{D(on)}$	$V_+ = +5.5\text{ V}$, $V_- = 0\text{ V}$ $V_D = V_S = 1\text{ V}/4.5\text{ V}$	Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	
Digital Control									
Input Current, V_{IN} Low	I_L	$V_{IN(A, B, C \text{ and } ENABLE)}$ Under Test = 0.8 V	Full	0.01	- 1	1	- 1	1	μA
Input Current, V_{IN} High	I_H	$V_{IN(A, B, C \text{ and } ENABLE)}$ Under Test = 2.0 V	Full	0.01	- 1	1	- 1	1	
Dynamic Characteristics									
Transition Time	t_{TRANS}	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ See Figure 1, 2, 3	Room Full	38		121 143		121 134	ns
Enable Turn-On Time	t_{ON}		Room Full	38		110 126		110 119	
Enable Turn-Off Time	t_{OFF}		Room Full	38		103 118		103 111	
Break-Before-Make Time Delay	t_D		Room Full	10		2		2	
Charge Injection ^e	Q	$V_g = 0\text{ V}$, $R_g = 0\ \Omega$, $C_L = 1\text{ nF}$	Full	0.5					pC
Off Isolation ^e	OIRR	$R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ $f = 100\text{ kHz}$	Room	< - 90					dB
Channel-to-Channel Crosstalk ^e	X_{TALK}		Room	< - 90					
Power Supplies									
Power Supply Current	I_+	$V_{IN(A, B, C \text{ and } ENABLE)} = 0\text{ or }5\text{ V}$	Room Full	0.05		1 10		1 10	μA
Negative Supply Current	I_-		Room Full	- 0.05	- 1 - 10		- 1 - 10		
Ground Current	I_{GND}		Room Full	- 0.05	- 1 - 10		- 1 - 10		



SPECIFICATIONS FOR UNIPOLAR SUPPLIES									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{CC} = +3\text{ V}$, $V_{EE} = 0\text{ V}$ $V_{IN(A, B, C \text{ and } ENABLE)} = 1.4\text{ V}$, 0.6 V^a	Temp. ^b	Typ. ^c	- 40 to 125 °C		- 40 to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	3	0	3	V
On-Resistance	R_{ON}	$I_S = 1\text{ mA}$, $V_D = 1.5\text{ V}$	Room Full	175		265 310		265 298	Ω
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = +3.3\text{ V}$, $V_- = 0\text{ V}$ $V_D = 0.3\text{ V}/3.0\text{ V}$, $V_S = 3.0\text{ V}/0.3\text{ V}$	Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	nA
	$I_{D(off)}$		Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	
Channel On Leakage Current	$I_{D(on)}$	$V_+ = +3.3\text{ V}$, $V_- = 0\text{ V}$ $V_D = V_S = 0.3\text{ V}/3.0\text{ V}$	Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	
Digital Control									
Input Current, V_{IN} Low	I_L	$V_{IN(A, B, C \text{ and } ENABLE)}$ Under Test = 0.6 V	Full	0.01	- 1	1	- 1	1	μA
Input Current, V_{IN} High	I_H	$V_{IN(A, B, C \text{ and } ENABLE)}$ Under Test = 1.4 V	Full	0.01	- 1	1	- 1	1	
Dynamic Characteristics									
Transition Time	t_{TRANS}	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ See Figure 1, 2, 3	Room Full	81		172 218		172 194	ns
Enable Turn-On Time	t_{ON}		Room Full	71		151 183		151 167	
Enable Turn-Off Time	t_{OFF}		Room Full	69		138 161		138 151	
Break-Before-Make Time Delay	t_D		Room Full	23		5		5	
Charge Injection ^e	Q	$V_g = 0\text{ V}$, $R_g = 0\ \Omega$, $C_L = 1\text{ nF}$	Room	0.5					pC
Off Isolation ^e	OIRR	$R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ $f = 100\text{ kHz}$	Room	< - 90					dB
Channel-to-Channel Crosstalk ^e	X_{TALK}		Room	< - 90					
Power Supplies									
Power Supply Current	I_+	$V_{IN(A, B, C \text{ and } ENABLE)} = 0\text{ or }3\text{ V}$	Room Full	0.05		1 10		1 10	μA
Negative Supply Current	I_-		Room Full	- 0.05	- 1 - 10		- 1 - 10		
Ground Current	I_{GND}		Room Full	- 0.05	- 1 - 10		- 1 - 10		

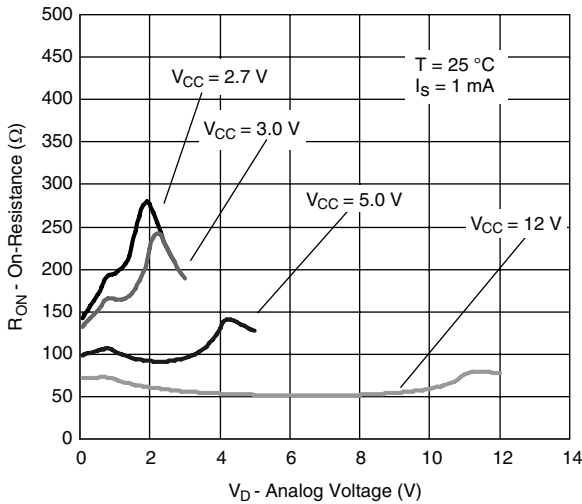
Notes:

- V_{IN} = input voltage to perform proper function.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.

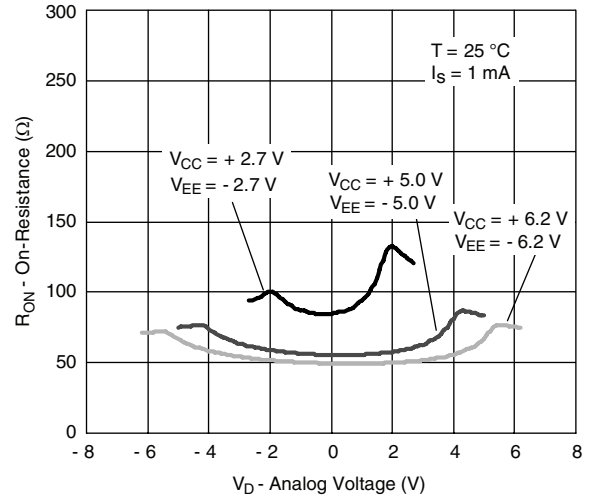
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



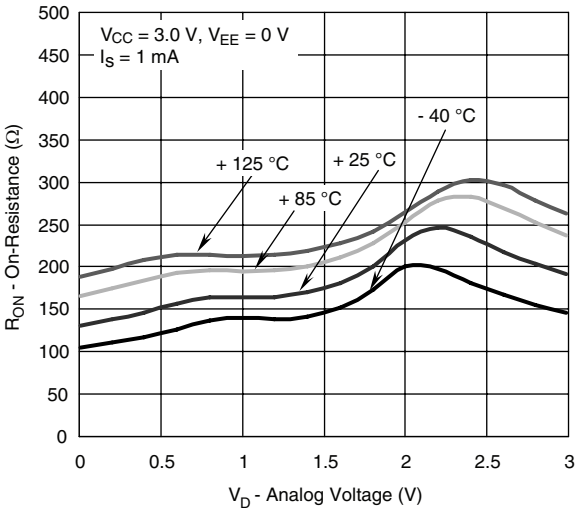
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



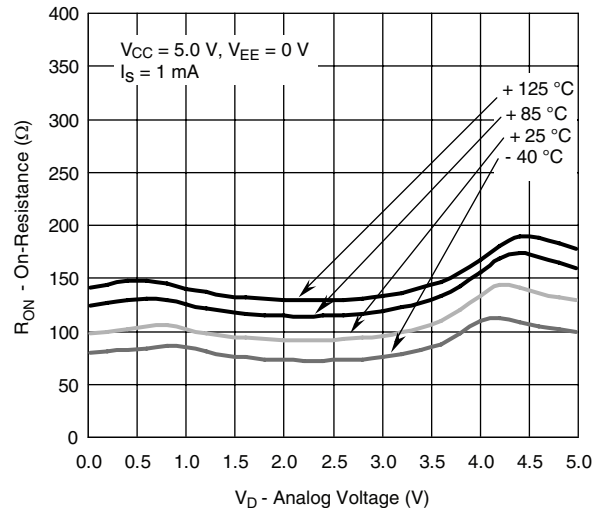
On-Resistance vs. V_D and Single Supply Voltage



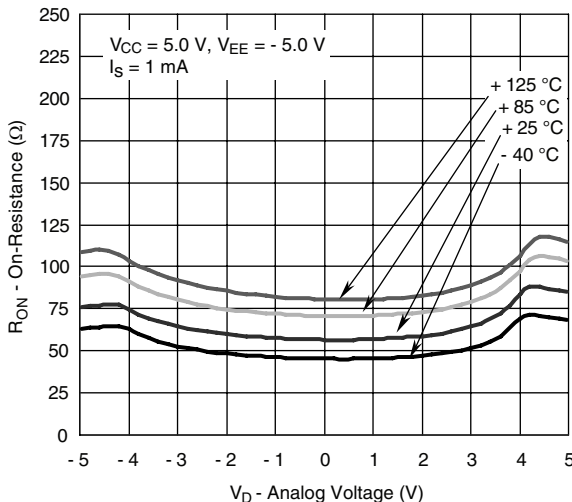
On-Resistance vs. V_D and Dual Supply Voltage



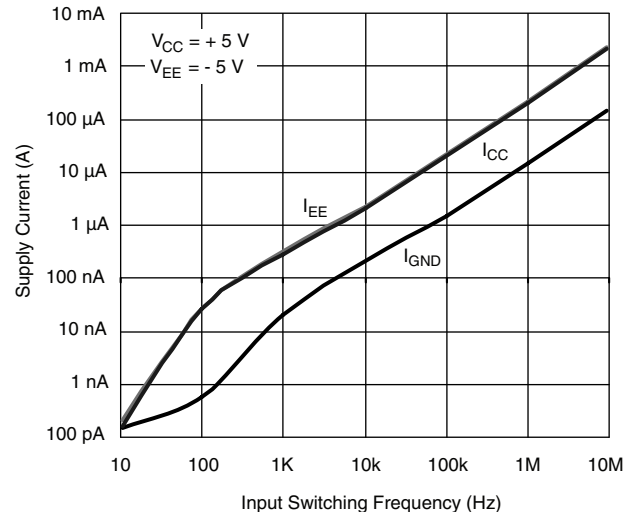
On-Resistance vs. Analog Voltage and Temperature at $V_{CC} = +3\text{ V}$, $V_{EE} = 0\text{ V}$



On-Resistance vs. Analog Voltage and Temperature at $V_{CC} = +5\text{ V}$, $V_{EE} = 0\text{ V}$



On-Resistance vs. Analog Voltage and Temperature at $V_{CC} = +5\text{ V}$, $V_{EE} = -5\text{ V}$



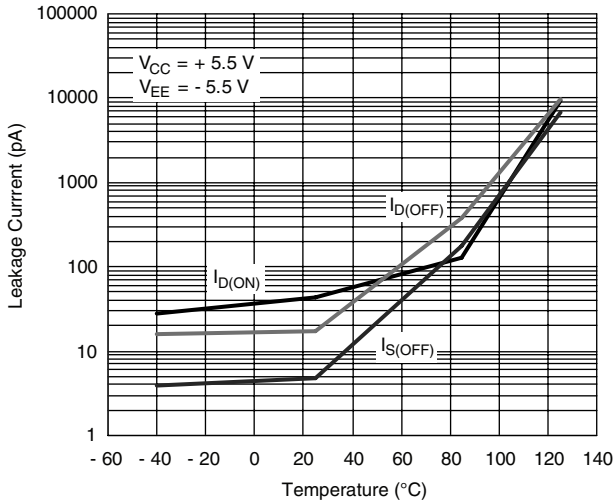
Supply Current vs. Input Switching Frequency

DG4051A/DG4052A/DG4053A

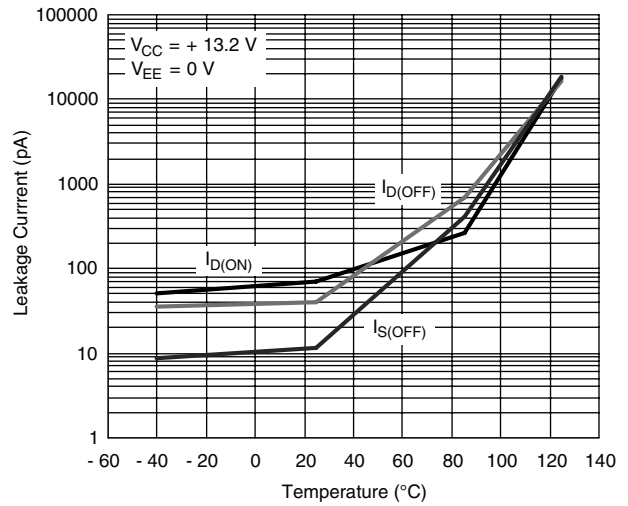


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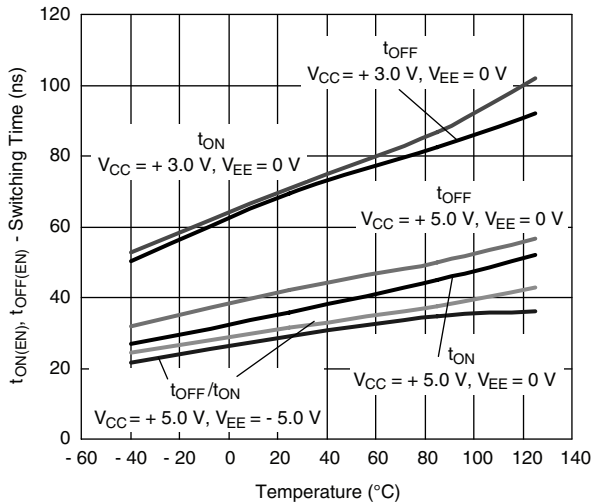
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



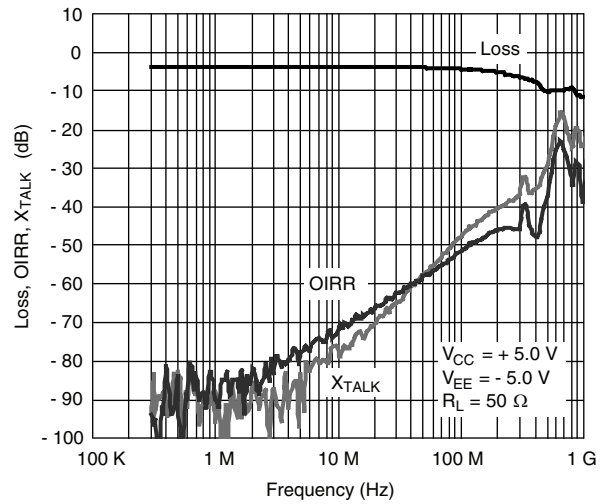
Leakage Current vs. Temperature



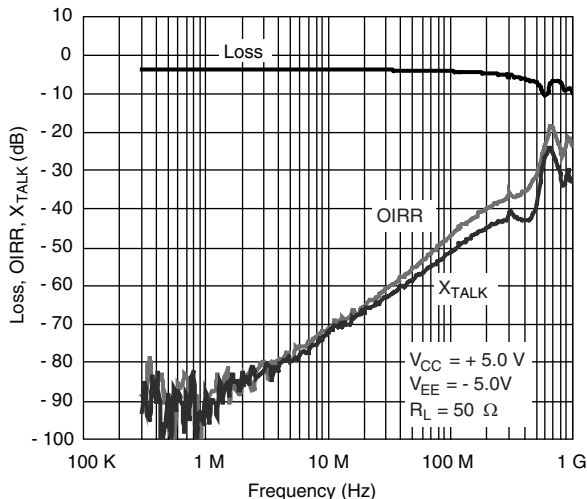
Leakage Current vs. Temperature



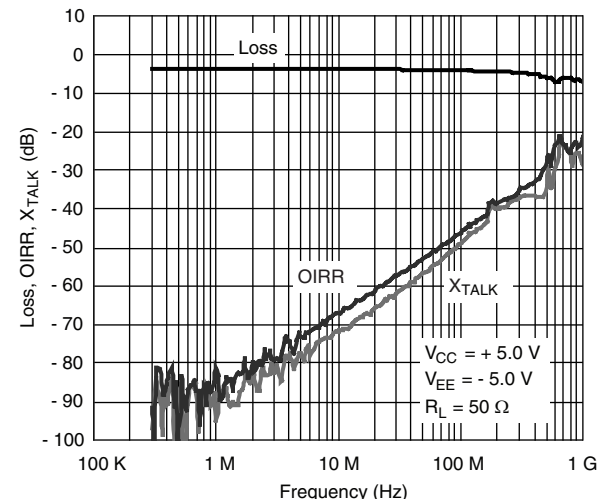
Switching Time vs. Temperature



DG4051A Insertion Loss, Off-Isolation, Crosstalk vs. Frequency at ± 5 V Supply



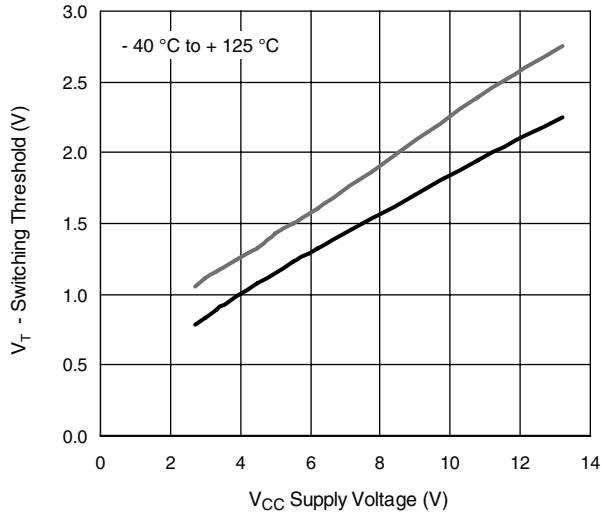
DG4052A Insertion Loss, Off-Isolation, Crosstalk vs. Frequency at ± 5 V Supply



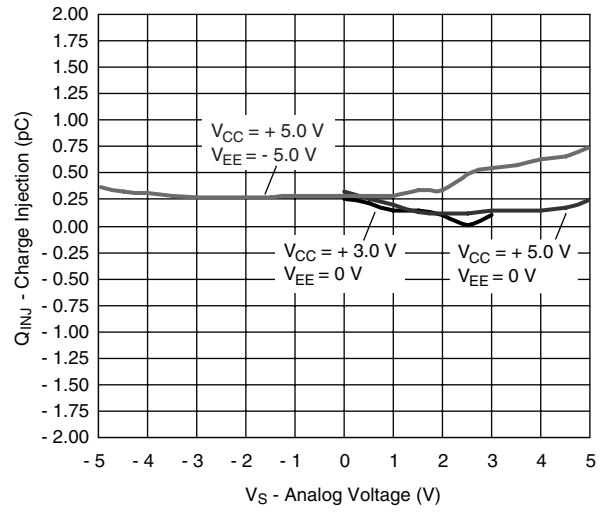
DG4053A Insertion Loss, Off-Isolation, Crosstalk vs. Frequency at ± 5 V Supply



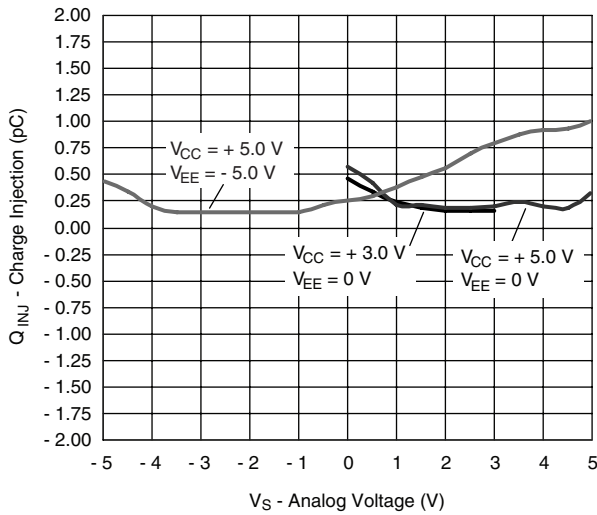
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



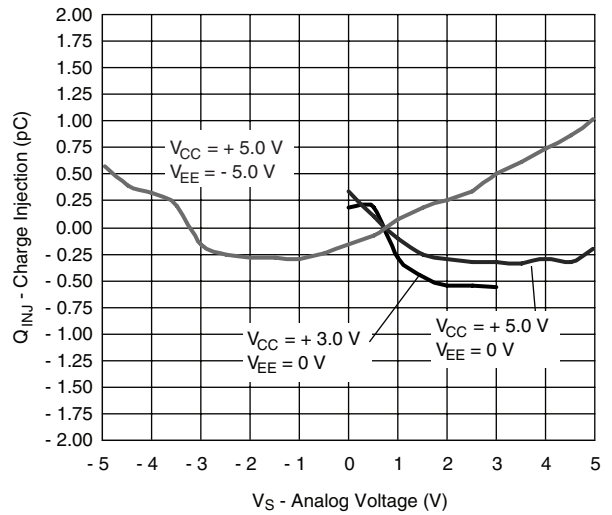
Switching Threshold vs. V_{CC} Supply Voltage



DG4051A Charge Injection vs. Analog Voltage



DG4052A Charge Injection vs. Analog Voltage



DG4053A Charge Injection vs. Analog Voltage

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TEST CIRCUITS

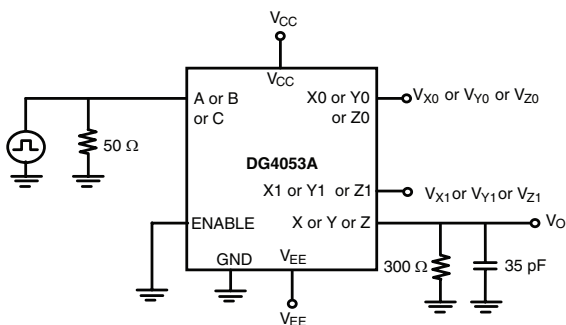
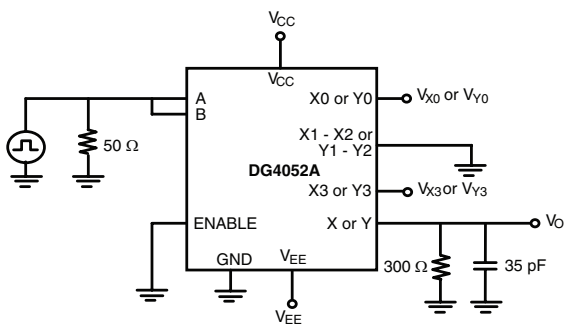
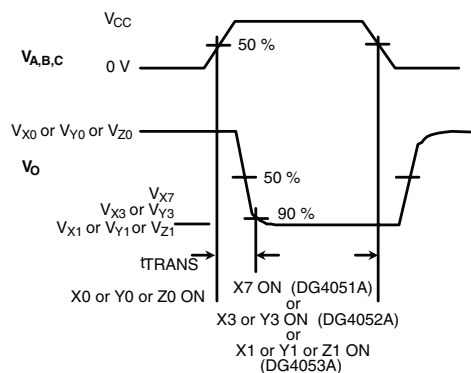
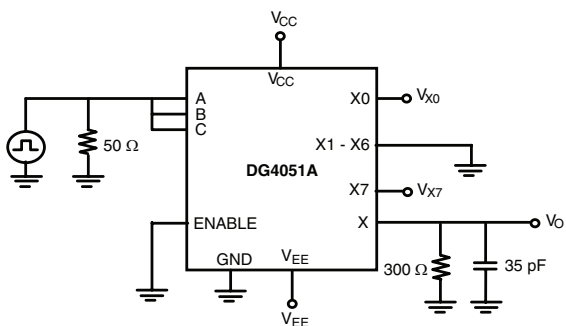


Figure 1. Transition Time

TEST CIRCUITS

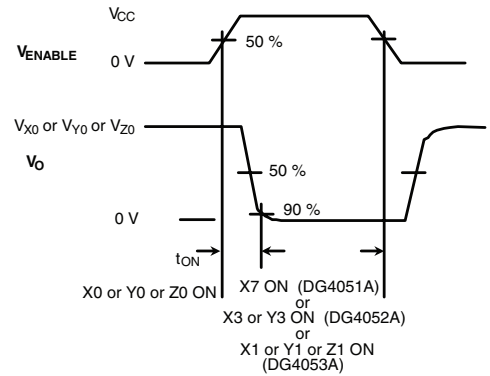
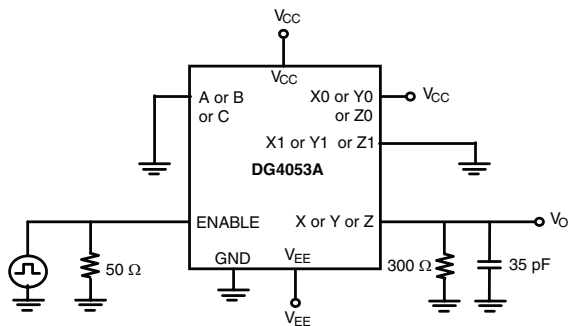
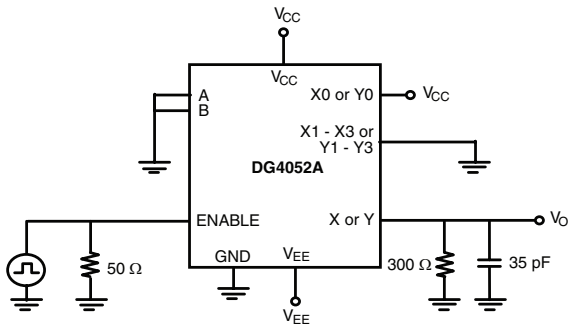
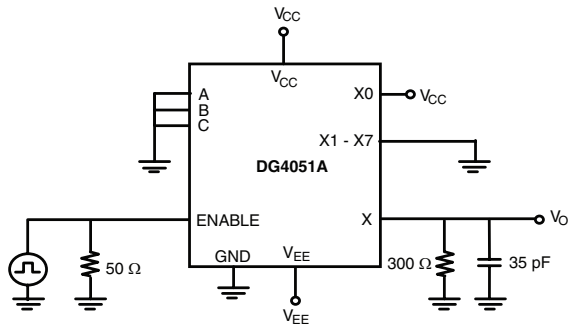


Figure 2. Enable Switching Time

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TEST CIRCUITS

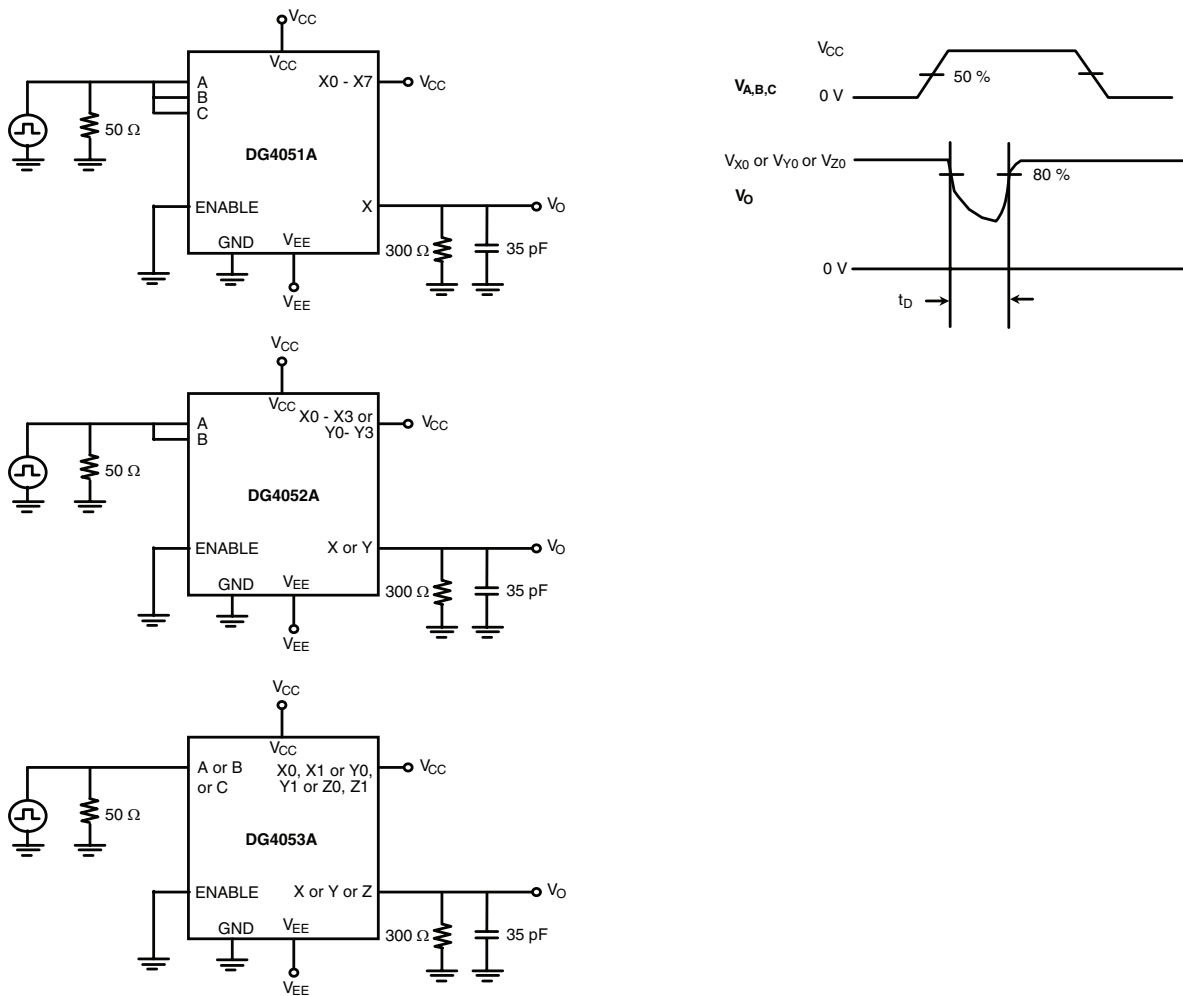


Figure 3. Break-Before-Make

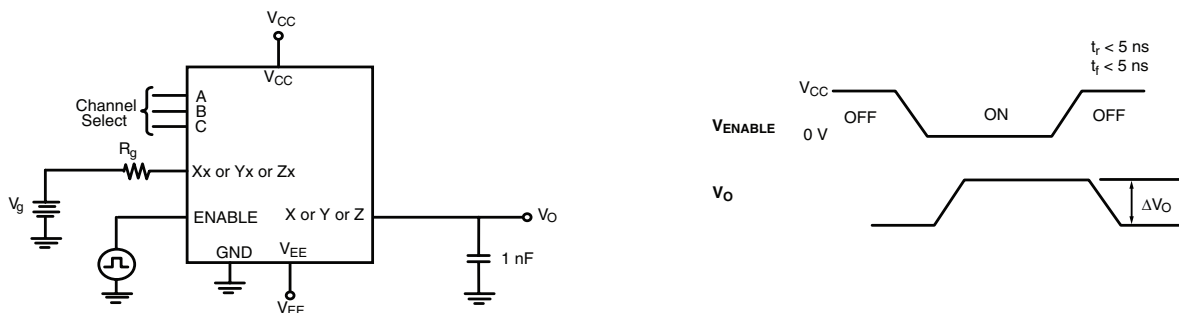
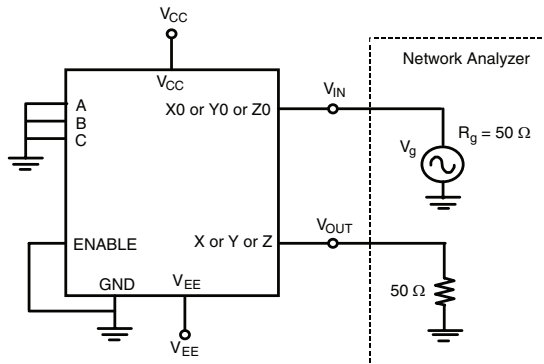


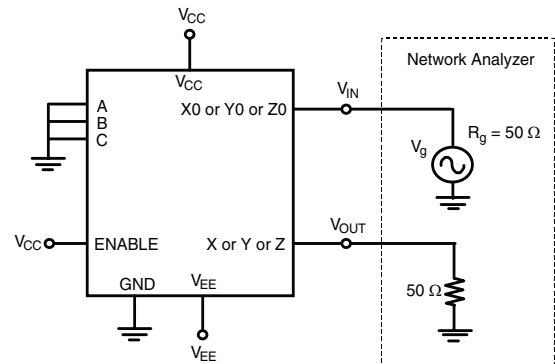
Figure 4. Charge Injection

TEST CIRCUITS



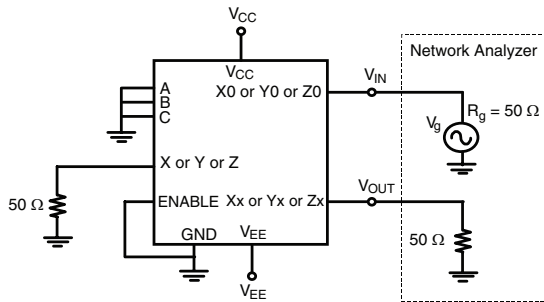
$$\text{Insertion Loss} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Figure 5. Insertion Loss



$$\text{Off Isolation} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Figure 6. Off Isolation



$$\text{Crosstalk} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Figure 7. Crosstalk

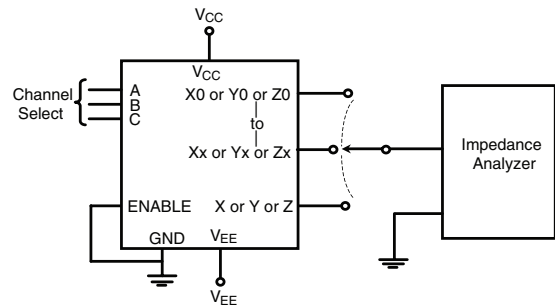


Figure 8. Source, Drain Capacitance

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